

(19) World Intellectual Property
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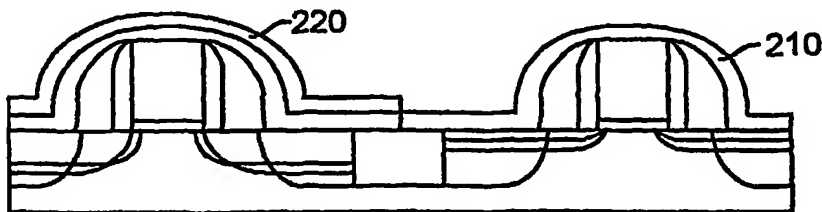
(43) International Publication Date
14 July 2005 (14.07.2005)

PCT

(10) International Publication Number
WO 2005/064665 A1

- (51) International Patent Classification?: **H01L 21/336**, 21/425, 27/01, 29/76, 29/167
- (21) International Application Number:
PCT/US2003/039025
- (22) International Filing Date: 8 December 2003 (08.12.2003)
- (25) Filing Language: English
- (26) Publication Language: English
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- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Declaration under Rule 4.17:**
— of inventorship (Rule 4.17(iv)) for US only
- Published:**
— with international search report
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: REDUCTION OF BORON DIFFUSIVITY IN pFETs



(57) Abstract: A stressed film applied across a boundary defined by a structure or a body (e.g. substrate or layer) of semiconductor material provides a change from tensile to compressive stress in the semiconductor material proximate to the boundary and is used to modify boron diffusion rate during annealing and thus modify final boron concentrations and/or profiles/gradients. In the case of a

field effect transistor, the gate structure may be formed with or without sidewalls to regulate the location of the boundary relative to source/drain, extension and/or halo implants. Different boron diffusion rates can be produced in the lateral and vertical directions and diffusion rates comparable to arsenic can be achieved. Reduction of junction capacitance of both nFETs and pFETs can be achieved simultaneously with the same process steps.